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REFERENCE DESIGN

IRMCS2033

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IRMCS2033

Low Voltage Sensorless Drive Design Platform for Permanent Magnet Motors

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
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IRMCS2033

Low Voltage Sensorless Drive Design Platform for Permanent Magnet Motors

Features

- **Low cost complete AC sensorless drive design platform**
- **IRMCK203 IC for complete sensorless control**
- **Simple design with IR2175 current sensing HVIC**
- **350W output power with MOSFET inverter**
- **Wide speed range and high speed operation**
- **Support any permanent magnet AC motors**
- **Low loss/EMI Space Vector PWM**
- **No phase voltage feedback sensing**
- **Low cost A/D interface with multiplexer**
- **4-channel D/A output for diagnostics/monitoring**
- **ServoDesigner™ tool for easy operation**
- **RS232C/RS422 and fast SPI interface**
- **Parallel interface for microcontroller expansion**
- **Over-current and ground fault protection**
- **Over-voltage / Under-voltage protection**
- **Dynamic Braking control with on-board brake resistor**
- **Discrete I/Os (START/STOP, FAULT, FLTCLR, SYNC, ESTOP, DIR, PWM Enable)**
- **Configuration data retention at power up/down**

Product Summary

Speed operation range (typical)	5 to 100%
High speed operation	100,000 rpm (2 pole)
Speed accuracy	0.01%
Speed resolution	15 bit
PWM carrier frequency	65 kHz max
Sensorless control computation time	10 usec
Input dc voltage range	22 to 50 V (typical)
Continuous output current	6 Arms @20KHz fPWM
Overload output current	18 Arms (3 secs)
Continuous output power	350 W
Max RS232C speed	57.6 kbps
Optional RS422 communication	1 Mbps

Description

IRMCS2033 is a Sensorless drive design platform for low voltage applications up to 350W output power. The system contains the latest advanced motion control IC, IRMCK203, and the ServoDesigner™ software. The complete B/Ms and schematics are provided so that the user can adapt and tailor the design per application needs. The system does not require any software code development due to the unique Motion Control Engine implemented in the IRMCK203 IC. Users can readily evaluate high performance Sensorless control without spending the development effort usually required in the traditional DSP or microcontroller based system. IRMCS2033 contains advanced iMOTION chipset such as IR2175 monolithic current sensing ICs and IRMCK203 full Sensorless Permanent Magnet motor drive, which enables simple and cost effective motion control design.

Overview

The IRMCS2033 is a low voltage drive design platform for a complete Sensorless Permanent Magnet motor drive system based on the IRMCK203 digital motion control IC. The system is based on a configurable control engine implemented by hardware logic in the IRMCK203. The system has a simple and low cost structure, made possible by advanced IR motion components including the IR2175 monolithic current sensing high voltage IC and IR2106 gate driver IC. Instead of using IR2175 as current feedback option, IRMC2033 also supports Inverter Low side shunt current feedback via A/D converter. These feedback options used in conjunction with the IRMCK203 simplify hardware implementation. Since all control logic is implemented in hardware logic as opposed to programmed software, unmatched parallel computation is achieved, resulting in higher bandwidth control and higher motor operating frequency (15 usec minimum PWM loop cycle).

Despite hardware logic implementation, its design flexibility allows the user to configure Permanent Magnetic ac motors (Sinusoidal Back EMF) with different motor parameters and different types of communication protocols.

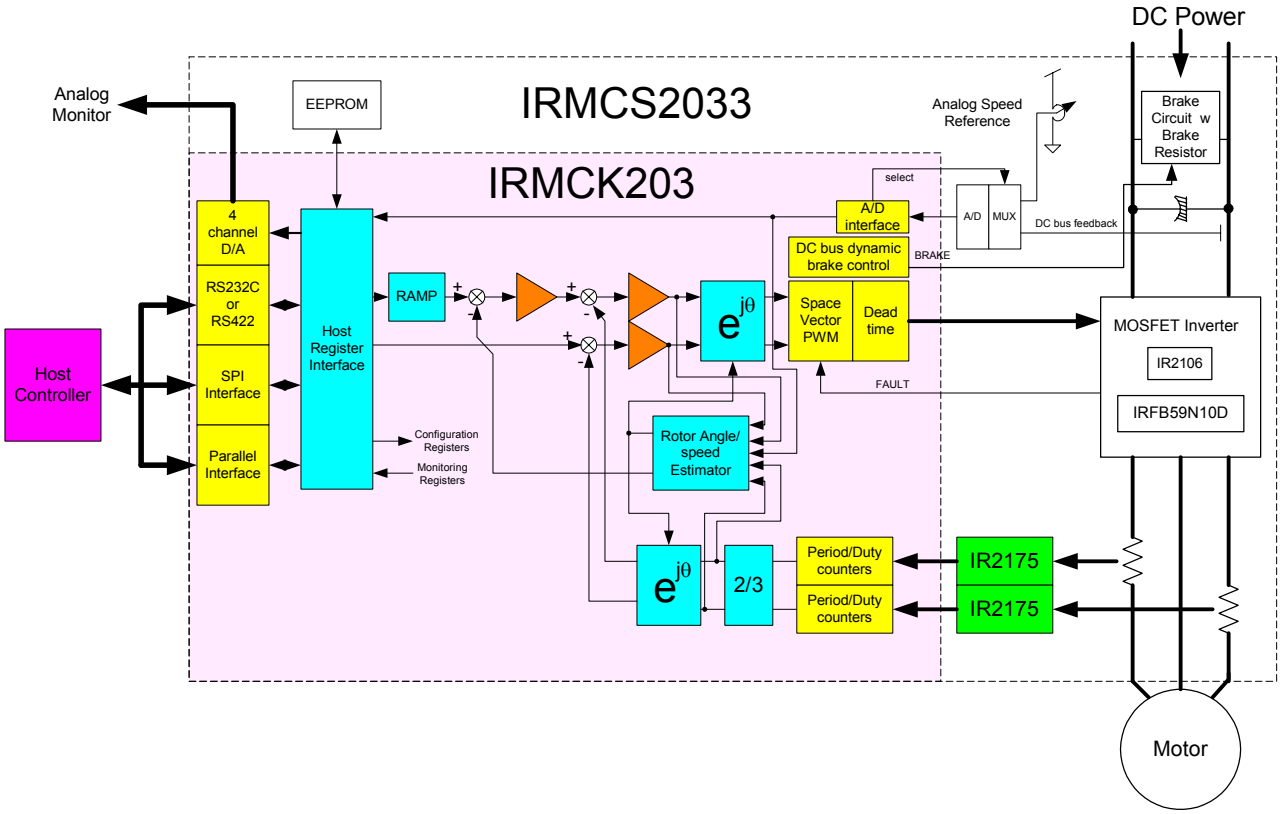


Figure 1. IRMCS2033 System Block Diagram

Safety Precautions

In addition to the precautions listed throughout this manual, please read and understand the following statements regarding hazards associated with AC servo development system.

ATTENTION: The ground potential of the IRMCS2033 system is biased to a negative DC bus voltage potential. When measuring voltage waveform by oscilloscope, the scope ground needs to be isolated. Failure to do so may result in personal injury or death.
Darkened display LEDs is not an indication that capacitors have discharged to safe voltage levels.

ATTENTION: The IRMCS2033 system contains dc bus capacitors which take time to discharge after removal of main supply. Before working on drive system, wait three minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death.
Darkened display LEDs is not an indication that capacitors have discharged to safe voltage levels.

ATTENTION: Only personnel familiar with the drive and associated machinery should plan or implement the installation, start-up, and subsequent maintenance of the system. Failure to comply may result in personal injury and/or equipment damage.

ATTENTION: The surface temperatures of the drive may become hot, which may cause injury.

ATTENTION: The IRMCS2033 system contains ESD (Electrostatic Discharge) sensitive parts and assemblies. Static control precautions are required when installing, testing, servicing or repairing this assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with static control procedures, reference applicable ESD protection handbook and guideline.

ATTENTION: An incorrectly applied or installed drive can result in component damage or reduction in product life. Wiring or application errors such as undersizing the motor, supplying an incorrect DC voltage, or excessive ambient temperatures may result in system malfunction.

ATTENTION: Remove dc power input to IRMCS2033 while disconnecting or reconnecting wires or performing service. Wait three minutes after removing power to discharge the bus voltage. Do not attempt to service the drive until bus voltage has discharged to zero. Failure to do so may result in bodily injury or death.

ATTENTION: Do not connect power factor correction capacitors to drive output terminals U, V, and W. Failure to do so may result in equipment damage or bodily injury.

Debris When Unpacking

The IRMCS2033 system is shipped with packing materials that need to be removed prior to installation.

ATTENTION: Failure to remove all debris and packing materials, which are unnecessary for system installation, may result in overheating or abnormal operating condition.

Hardware Installation

Check All Hardware

The following hardware pieces are contained in the IRMCS2033 system.

- IRMCS2033 board with integrated heat sink
- Serial RS232C cable with 9-pin Dsub connectors for ServoDesigner™ development tool
- Two 10 m Ohms shunt resistors

Installation Procedure

Step 1.
Visually inspect IRMCS2033 board to check for loose wiring, loose or damaged components or other abnormalities.

Step 2.
Connect Motor cable and DC power to IRMCS2033 J1 connector.

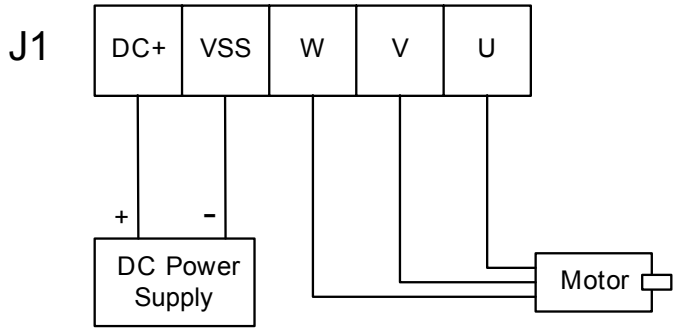
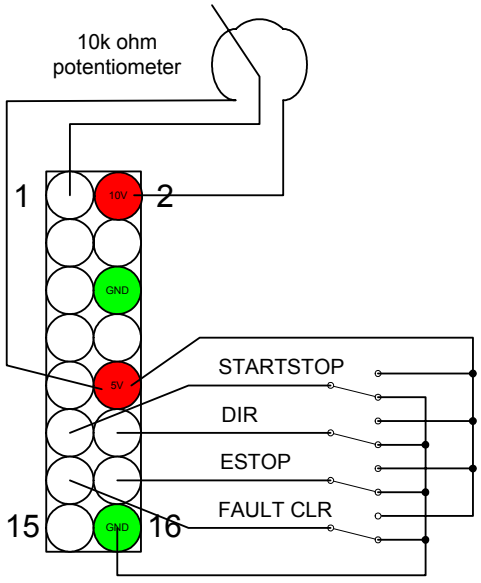


Figure 2. Power Connector, J1

Step 3. (Optional) J6 Connector RS232C
Connect the RS232C cable between 9-pin D-sub connector and PC.

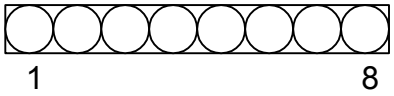
Step 4. (Optional) J7 Connector, External I/O
Connect External I/O Connector (J7) as needed. All inputs are 5V tolerant.



Pin Definition
Pin 1: Analog speed reference input
Pin 2: +10V
Pin 3: N/A (open)
Pin 4: N/A (open)
Pin 5: N/A (open)
Pin 6: GND
Pin 7: FAULT status output (high when FAULT)
Pin 8: SYNC status output (2 usec width of active low pulse at every carrier frequency period)
Pin 9: PWM Enable status output (high when PWM is enabled)
Pin 10: +5V
Pin 11: STARTSTOP input (positive edge transition to start; negative edge transition to stop)
Pin 12: DIR input (high = fwd; low = rev)
Pin 13: ESTOP input (high to activate emergency stop)
Pin 14: FAULT CLR input (1usec pulse to clear fault)
Pin 15: N/A (open)
Pin 16: GND

Figure 3. J7 Connector

Step 5. (Optional) J8 Connector, Analog Output monitoring



J8 Top View

Figure 4. J8 Connector

Pin Definition
Pin 1: Channel 1 Analog output (0-5V)
Pin 2: GND
Pin 3: Channel 2 Analog output (0-5V)
Pin 4: GND
Pin 5: Channel 3 Analog output (0-5V)
Pin 6: GND
Pin 7: Channel 4 Analog output (0-5V)
Pin 8: GND

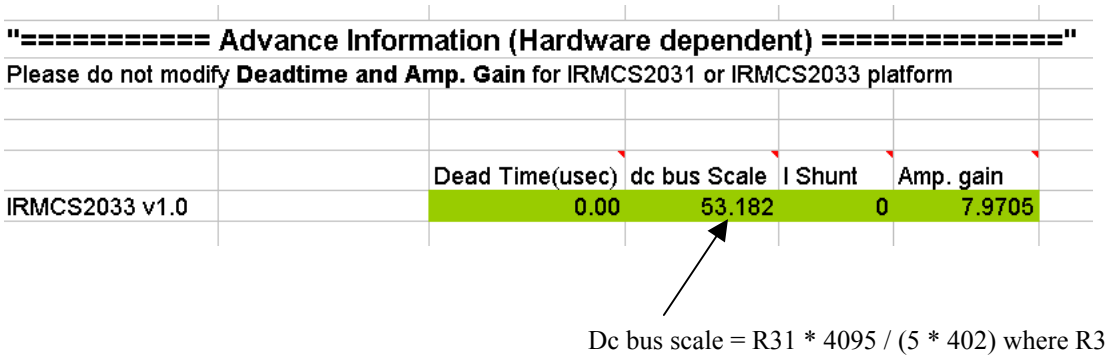
Step 6. (Optional) Rescale bus voltage range

The default voltage levels are:
Over voltage trip = 63.2 V
Under voltage trip = 18.4 V
Dynamic brake voltage = 58.7V

If a different voltage range is desired, the user can modify hardware (resistors) to obtain a different voltage range. Resistors R31 and R43 (R31 = R43) can be replaced to accommodate a different voltage range.

Over voltage trip = 402 / R31 * 5 * 3360 / 4095 volts **(must not exceed 70 Volts)**
Under voltage trip = 402 / R31 * 5 * 976 / 4095 volts **(must be above 15 Volts)**
Dynamic brake voltage = 402 / R31 * 5 * 3120 / 4095 volts

After determining the value of R31 (R43 = R31), the dc bus scaling in the Excel Spreadsheet (drive commissioning tool) need to be updated by the following equation:



Dc bus scale = R31 * 4095 / (5 * 402) where R31 is in **Kohm.**

Installing the Software

The ServoDesigner™ tool is distributed on the CD-ROM. Load the CD into the CD-ROM drive on a PC and double-click “IRMCS2033.exe”. The installation requires a password, which can be found in the file “iMOTION Install IRMCS2033.pdf” on the same CD-ROM. The automated procedure installs all necessary software on the PC. The default location for the installation is “C:\Program Files\iMOTION”.

Power-On the System

Apply DC power 20 to 45V (recommended voltage range) to the system (IRMCS2033).

Immediately after power-on, the LED will turn green indicating successful configuration of the IRMCK203.

Getting Started

For quick start with preconfigured parameters, the following motor is supported with a preconfigured motor file.

- Maxon 118889 (80W, 11000rpm)

If any other motor is used, reconfiguration is required. Configurable parameters are required to tailor the design to various applications (motor and load). These configurable parameters can be modified via the host register interface (using the ServoDesigner tool) through the communication interface. In the IRMCS2033 product, a design spreadsheet (Drive parameters translator) is provided to aid the user for ease of drive start-up. Using the spreadsheet, the user enters high-level parameters such as motor nameplate information, maximum application speed, current limit, and speed regulator bandwidth. This high-level user information is translated to engineering parameters (directly used by the drive). Figure 5 gives an overview of the commissioning steps. Please refer to the IRMCK203 Application Developer's Guide for a detailed description of drive commissioning.

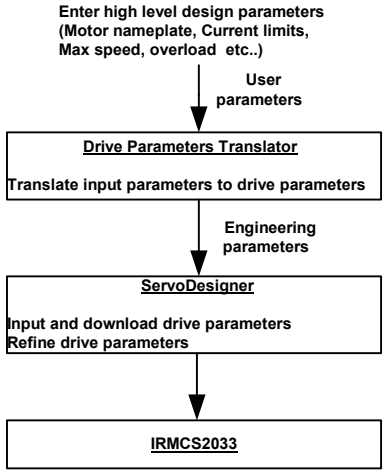


Figure 5. Overview of Drive Commissioning

Shunt Resistor and Current Rating

Two 20m Ohms current sensing shunt resistors are equipped as default resistors at factory shipment (R11 and R12 located on the top side of PCB). With these resistors, IRMCS2033 can deliver up to ±13A maximum peak current (using IR2175) to the motor including overshoot of current regulation when using IR2175 as current feedback.

IRMCS2033 motor commissioning tool (IRMCS2033-DriveParams.xls) will calculate the appropriate resistor value for a particular peak Ampere requirement.

RS232C connector

IRMCS2033 has one serial RS232C connector (J6) on the board. The connector is a D-sub 9 pin standard PC female connector and directly connectable to a PC serial port. As shown in Figure 6, pin 2 is the send signal and pin 3 is the receive signal; both are 10V signal level. The baud rate is fixed at 57.6kbps. The signal format is 8 bits, no parity, 1 stop bit configuration.

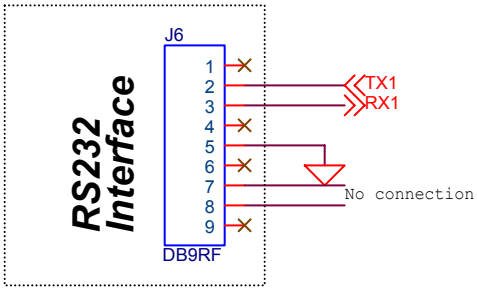


Figure 6. RS232C Connector

RS-232 Register Access

The IRMCK203 includes an RS-232 interface channel that provides a direct connection to the host PC. The software interface combines a basic "register map" control interface with a simple communication protocol to accommodate potential communication errors. For more detailed information, please refer to the IRMCK203 Application Developer's Guide.

RS-232 Register Write Access

A Register write operation consists of a command/address byte, byte count, register data and checksum. When the IRMCK203 receives the register data, it validates the checksum, writes the register data, and transmits and acknowledgement to the host.

Command / Address Byte	Byte Count	1-6 bytes of register data	Checksum

Register Write Operation

Command Acknowledgement Byte	Checksum

Register Write Acknowledgement

Bit Position							
7	6	5	4	3	2	1	0
1=Read/ 0=Write	Register Map Starting Address						

Command/Address Byte Format

Bit Position							
7	6	5	4	3	2	1	0
1=Error/ 0=OK	Register Map Starting Address						

Command Acknowledgement Byte Format

The following example shows a command sequence sent from the host to the IRMCK203 requesting a two-byte register write operation:

0x2F	Write operation beginning at offset 0x2F
0x02	Byte count of register data is 2
0x00	Data byte 1
0x04	Data byte 2
0x35	Checksum (sum of preceding bytes, overflow discarded)

A good reply from the IRMCK203 would appear as follows:

0x2F	Write completed OK at offset 0x2F
0x2F	Checksum

An error reply to the command would have the following format:

0xAF	Write at offset 0x2F completed in error
0xAF	Checksum

RS-232 Register Read Access

A register read operation consists of a command/address byte, byte count and checksum. When the IRMCK203 receives the command, it validates the checksum and transmits the register data to the host.

Command / Address Byte	Byte Count	Checksum

Register Read Operation

Command Acknowledgement Byte	Register Data (Byte Count bytes)	Checksum

Register Read Acknowledgement (transfer OK)

Command Acknowledgement Byte	Checksum

Register Read Acknowledgement (error)

The following example shows a command sequence sent from the host to the IRMCK203 requesting four bytes of read register data:

0xA0	Read operation beginning at offset 0x20 (high-order bit selects read operation)
0x04	Requested data byte count is 4
0xA4	Checksum

A good reply from the IRMCK203 might appear as follows:

0x20	Read completed OK at offset 0x20
0x11	Data byte 1
0x22	Data byte 2
0x33	Data byte 3
0x44	Data byte 4
0xCA	Checksum

An error reply to the command would have the following format:

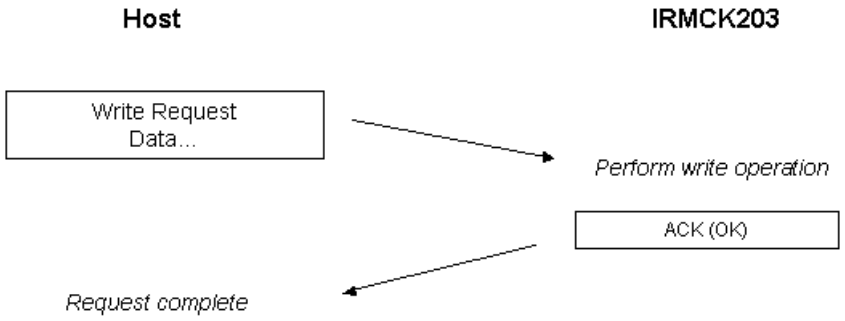
0xA0	Read at offset 0x20 completed in error
0xA0	Checksum

RS-232 Timeout

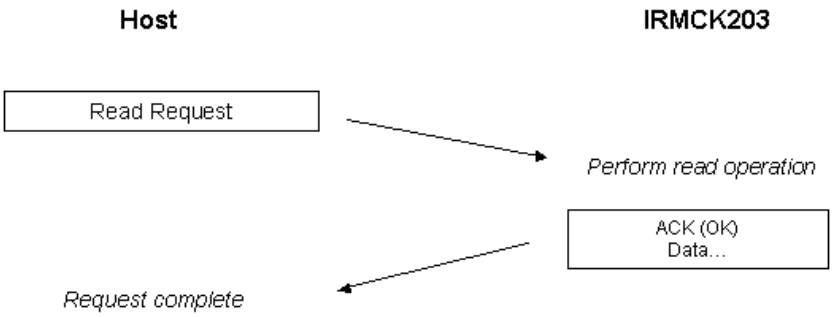
The IRMCK203 receiver includes a timer that automatically terminates transfers from the host to the IRMCK203 after a period of 32 msec.

RS-232 Transfer Examples

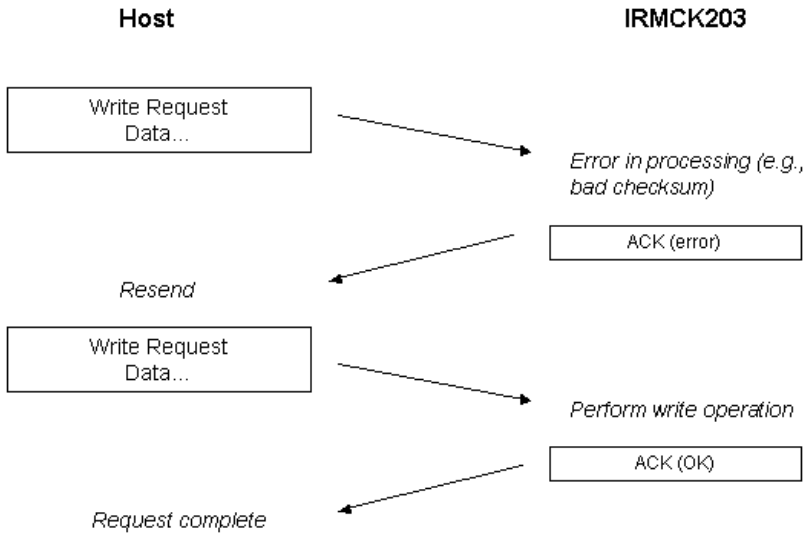
The following example shows a normal exchange executing a register write access.



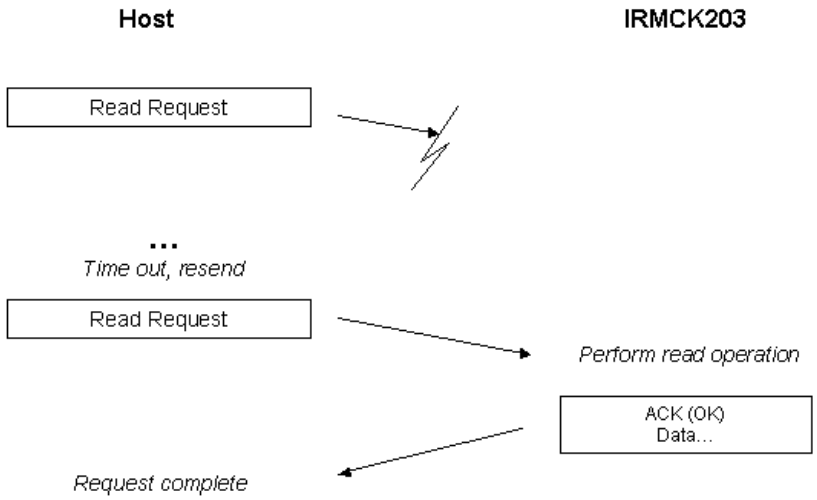
The example below shows a normal register read access exchange.



The following example shows a register write request that is repeated by the host due to a negative acknowledgement from the IRMCK203.



In the final example, the host repeats a register read access request when it receives no response to its first attempt.



SPI interface Connector

IRMCS2033 has one SPI interface connector (J4) on the board. The connector is a 6-pin header and its pin assignments are shown below. The signal level is 3.3V with 5V tolerant input. Maximum transmission speed is 6 MHz.

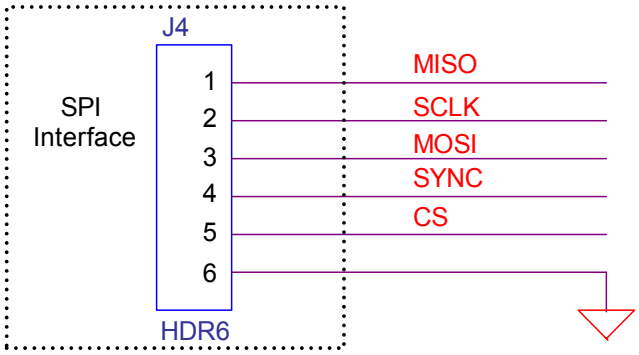


Figure 7. SPI Interface Connector

SPI Register Access

When configured as an SPI device read only and read/write operations are performed using the following transfer format:

Command Byte	Data Byte 0	.....	Data Byte N

Data Transfer Format

Bit Position							
7	6	5	4	3	2	1	0
Read Only	Register Map Starting Address						

Command Byte Format

Data transfers begin at the address specified in the command byte and proceed sequentially until the SPI transfer completes. As in the Host Parallel Access, the internal address register is incremented after each SPI byte is transferred. Note that accesses are read/write unless the “read only” bit is set.

Parallel Interface Port

IRMCS2033 provides an 8-bit parallel interface port to facilitate microprocessor interface. The interface is generic and compatible with most common 8-bit parallel interfaces such as MCS8051, some Motorola 8-bit uP, Microchip, etc. Figure 8 shows the connection diagram. The connector, J5, is a 2-by-10 header connector.

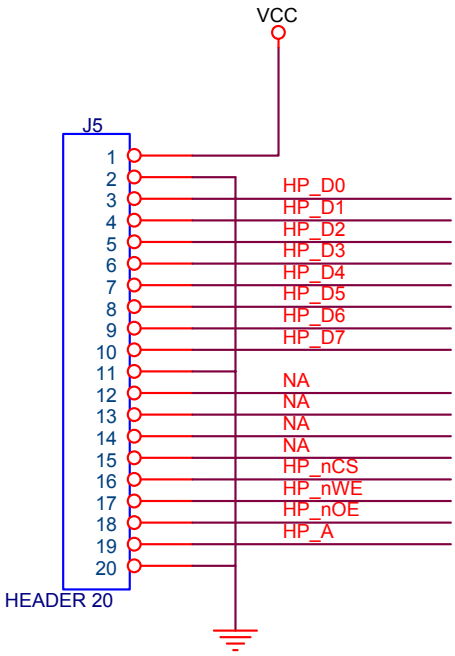


Figure 8. Parallel Interface Port

Each signal is 3.3V level and the data bus is multiplexed. Table 1 summarizes each signal definition.

Signal	I/O[1]	Description
HP_nCS	I	Active low Host Port Chip Select
HP_nOE	I	Active Low Host Port Output Enable
HP_nWE	I	Active low Host Port Write Enable
HP_A	I	Host Port Register Address. 1 = Address register, 0 = Data Register
HP_D*n*	I/O	Bidirectional Host Port data bus, where *n* = data bit 0 - 7

Table 1. Microprocessor Interface Module Signal Definitions

The IRMCK203 contains an address register that is updated with the Host Register address when HP_A = 1. After each subsequent data byte is either read or written, the internal address register is incremented. The diagram below shows that Data Bytes 0 to N would access register locations initially specified by the Address Byte. The Address Byte with the HP_A signal can be asserted at any time.

Address Byte	Data Byte 0	.....	Data Byte N
HP_A = 1	HP_A = 0	HP_A = 0	HP_A = 0

Host Parallel Data Transfer Format

Figure 9 and Table 2 show read cycle timing for the host parallel interface. Figure 10 and Table 3 show write cycle timing.

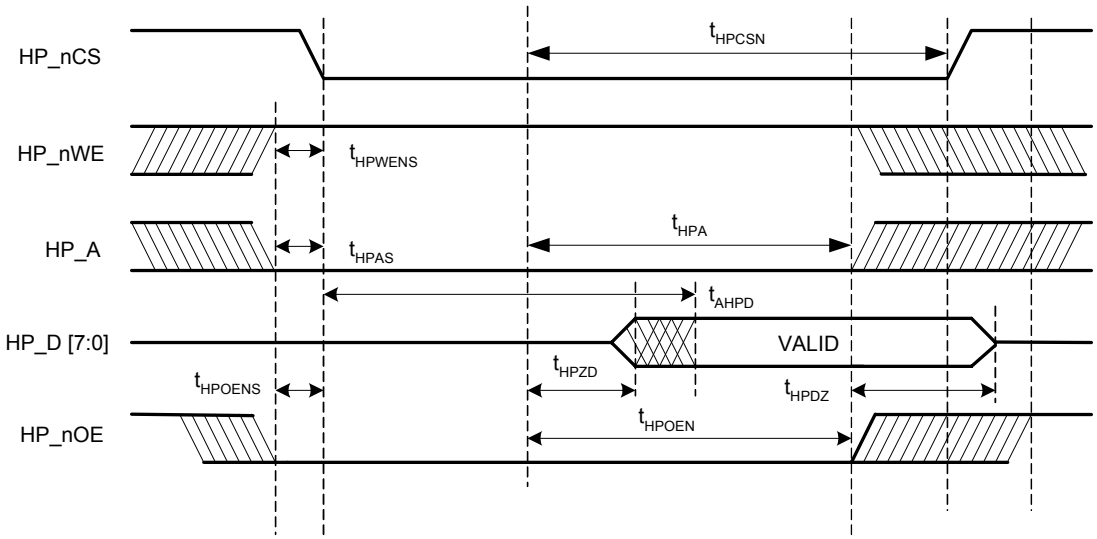


Figure 9. Host Parallel Read Cycle Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTE
t_{HPCSN}	HP_nCS Period	70		ns	
t_{HPWENS}	HP_nWE Setup	40		ns	Note 3
t_{HPAS}	HP_A Setup	40		ns	
t_{AHPD}	HP_D [7:0] Access	60	105	ns	
t_{HPZD}	HP_D [7:0] Active	0	9	ns	
t_{HPDZ}	HP_D [7:0] High Impedance	0	6	ns	
t_{HPOENS}	HP_nOE Setup	40		ns	Note 3
t_{HPOEN}	HP_nOE Period	70		ns	

Table 2: Host Parallel Read Cycle Timing

Note:
1. HP_nOE, HP_nWE must be stable before the high to low transition of HP_nCS.

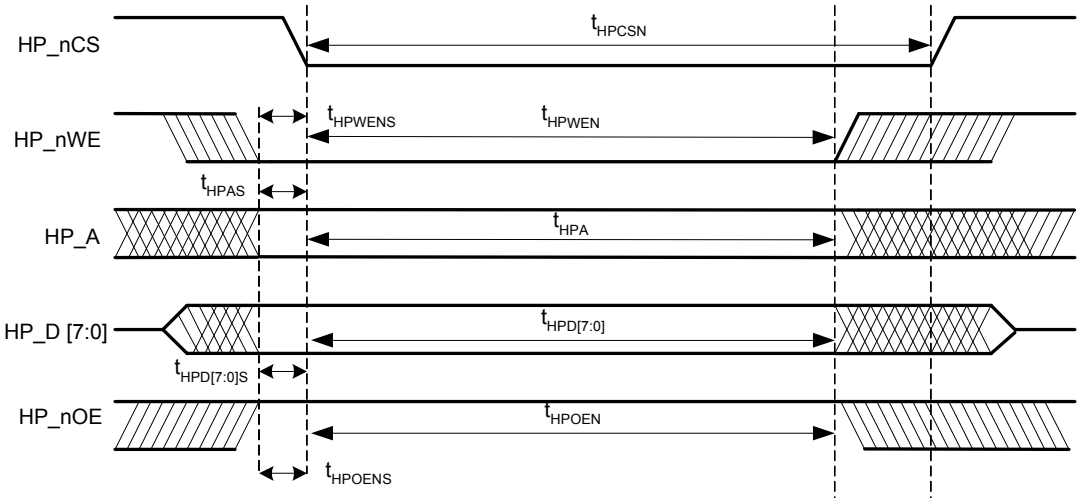


Figure 10. Host Parallel Write Cycle Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTE
t_{HPCSN}	HP_nCS Period	70		ns	
t_{HPWENS}	HP_nWE Setup	40		ns	
t_{HPWEN}	HP_nWE Period	70		ns	
t_{HPAS}	HP_A Setup	-10		ns	
t_{HPA}	HP_A Period	70		ns	
$t_{HPD[7:0]}$	HP_D [7:0] Setup	-10		ns	
t_{HPOENS}	HP_nOE Setup	40		ns	
t_{HPOEN}	HP_nOE Period	70		ns	Note 4

Table 3: Host Parallel Write Cycle Timing

Note:

2. HP_nOE must be asserted high while HP_nCS low during a Host Parallel Write Cycle.

Specifications

T_C = 25°C unless specified

Parameters	Values	Conditions
Voltage Level		
dc bus voltage range	22 to 50V	Maximum limited by Dynamic brake voltage
Over voltage trip	63.2V	Re-scalable by R31 and R43 (70V max)
Under voltage trip	18.4V	Re-scalable by R31 and R43 (15V min)
Dynamic brake voltage	58.7V	Re-scalable by R31 and R43
Output Power		
Watts	350W continuous power	fPWM = 20kHz, TA = 40°C, RthSA = 1.0 °C/W
Current	6 Arms nominal, 18 Arms Overload	3 secs overload
Host interface (SPI)		
SCLK,CS,MISO,MOSI, SYNC	3.3V logic level	maximum 6MHz
Host interface (RS232C)		
SND,RCV	10V	Maximum 57.6k bps, single ended, configurable for RS422 up to 1Mbps
Host interface (Parallel Port)		
HP_nCS,HP_nOE,HP_nWE, HP_A,HP_DATA[8]	3.3V	8 bit parallel interface compatible with 8051, Microchip, other uP.
D/A		
8- bit 4 Channel	0-3.3V output	Output are buffered with 4mA drive capability
A/D		
12-bit	DC bus, Speed Ref and Leg shunt current inputs	ADS7818 compatible
Discrete I/O		
Input	START/STOP, ESTOP, DIR, FLTCLR	5V tolerant, Active High logic
Output	PWMEnable, FAULT, SYNC	
Current feedback		
Current sensing device	IR2175, direct interface	
Resolution	10 bit (7.5 nanoseconds counting resolution)	133 MHz internal IRMCK203 clock
Latency	8.3 usec	2175 PWM output (120 kHz)
Protection		
Output current trip level	28A peak, ±10%	Detection from low side Leg Shunts
Ground fault trip level	28A peak, ±10%	Detection from positive dc bus
Short circuit delay time	2.5 usec	line-to-line short, line-to-DC bus (-) short
Power Device		
IRFB59N10D	6 MOSFETs	
System environment		
Ambient temperature	0 to 40°C	95% RH max. (non-condensing)

Table 4. IRMCS2033 Electrical Specification

International
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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 252-7105
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